HIGH DENSITY 3D RAIL STACK ARRAYS AND METHOD OF MAKING

FIELD OF THE INVENTION

TTN This application is a Div of 10/180,046 6/27/2002 PAT 6,737,675

[0001] The present invention is directed generally to semiconductor devices and methods of fabrication and more particularly to three dimensional arrays of thin film transistors and method of fabrication.

BACKGROUND OF THE INVENTION

[0002] Thin film transistors (TFTs) are utilized in various devices, such as a liquid crystal displays, static random access memories (SRAMs) and in nonvolatile memories. Conventional TFTs have a structure that is similar to conventional bulk metal oxide semiconductor field effect transistors (MOSFETs), except that TFTs are formed in a semiconductor layer that is located above an insulating substrate, such as a glass substrate or a semiconductor substrate that is covered by an insulating layer. The TFT device density on the substrate is usually lower than desired. The decreased device density increases the device cost, since fewer devices can be made on each substrate. PCT published application WO 02/15277 A2, which corresponds to U.S. Application Serial No. 09/927,648 filed on August 13, 2002, incorporated herein by reference in its entirety, describes how three dimensional rail stack arrays of TFTs may be used utilized to decrease device density.

BRIEF SUMMARY OF THE INVENTION

[0003] One preferred aspect of the present invention provides a semiconductor device, comprising a first field effect transistor, comprising (i) a first rail comprising a first channel, a first gate insulating layer and a first gate electrode, (ii) a first source region, and (iii) a first drain region.

electrode of said first transistor and the source of said second transistor are disposed in a portion of a first rail.

[0011] Another preferred aspect of the present invention provides a semiconductor device a semiconductor device comprising a first rail, the first rail comprising a gate electrode of a first field effect transistor, and a source or drain of a second field effect transistor. The first transistor and the second transistor are oriented in non-parallel directions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 is a three dimensional view of an array of the first preferred embodiment of the present invention.

[0013] Figures 2-3 are three dimensional views of portions of the array of the first preferred embodiment of the present invention.

[0014] Figures 4-7 are schematic diagrams illustrating how various circuit elements can be made using the array of the first preferred embodiment.

[0015] Figures 8 and 9 are three dimensional views of an array of the second preferred embodiment of the present invention.

[0016] Figures 10A-D are side cross sectional views of steps in a method of making of an array of the preferred embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] The present inventors have realized that the device density may be further increased in a rail stack array of TFTs if one rail is contains a gate of one TFT and a source/drain of another TFT.